1   1.   A method of operating a programmable logic integrated circuit

2   comprising:

3   loading an initial value in a count register of a watchdog timer circuit of the

4   programmable logic integrated circuit;

5   clocking the count register to advance the count register to a next value with each

6   clock;

7   periodically reloading the count register with the initial value;

8   when the stored count value held in the count register of the watchdog timer

9   circuit reaches a final value, asserting a triggered signal output; and

10   upon receiving the triggered signal output in a reset logic block of the

11   programmable logic integrated circuit, causing reloading of configuration data from an external

12   source into the programmable logic integrated circuit.

1   2.   The method of claim 1 wherein the external source is a nonvolatile

2   memory.

1   3.   The method of claim 1 wherein the external source is a serial EPROM.

1   4.   The method of claim 1 wherein the final value causes an overflow

2   condition for the count register of the watchdog timer circuit.

1   5.   The method of claim 1 wherein the watchdog timer circuit increments the

2   stored count value at each clock pulse.

1   6.   The method of claim 1 wherein the watchdog timer circuit decrements the

2   stored count value at each clock pulse.

1   7.   The method of claim 1 wherein periodically reloading the count register

2   comprises:

3   writing a magic value into a reload register of the watchdog timer circuit; and

4   when the magic value is received in the reload register, resetting the count register

5   of the watchdog timer circuit to the initial value.

1   8.   The method of claim 1 wherein periodically reloading the count register

2   comprises:

3   writing a first magic value into a reload register of the watchdog timer circuit;

4   when the first magic value is received in the reload register, reloading the count

5   register of the watchdog timer circuit to the initial value; and

6   after the first magic value is received in the reload register, permitting a

7   subsequent reload of the count register when a second magic value is written into reload register.

1   9.   The method of claim 8 further comprising:

2   continually reloading the count register to the initial value by writing the first and

3   second magic values to the reload register in sequence, alternately.

1   10.   The method of claim 1 further comprising:

2   using the configuration data to configure an embedded processor portion and a

3   programmable logic portion of the programmable logic integrated circuit.

1   11.   The method of claim 1 wherein to avoid asserting the triggered signal

2   output, a periodic reload of the watchdog timer circuit should be performed during a time period

3   it takes the watchdog timer circuit to count from the initial value to the final value.

1   12.   The method of claim 11 wherein the period is less than about two minutes.

1   13.   The method of claim 11 wherein the time period depends on clock

2   frequency used to clock the watchdog timer circuit.

1   14.   The method of claim 1 wherein the initial value is 0 and the final value is a

2   maximum count value permitted by the count register.

1   15.   The method of claim 1 wherein the count register comprises 32 bits.

1   16.   A method of designing a programmable logic integrated circuit

2   comprising:

3   taking a first layout of a programmable logic integrated circuit;

4   stretching the first layout using an edge of the first layout so the first layout has a

5 stretched section;

6   taking a second layout of an embedded processor stripe for a programmable logic

7 integrated circuit, wherein the embedded processor stripe comprises a watchdog timer circuit;

8   incorporating the second layout into stretched section of the first layout; and

9   coupling signal lines of the first layout to signal lines of the second layout.

1   17. The method of claim 16 further comprising:

2   fabricating the programmable logic integrated circuit using a combination of the

3 first and second layouts.

1   18. A programmable logic integrated circuit designed according to the method

2 recited in claim 16.

1   19. A method comprising:

2   designing a layout of an embedded processor stripe to be incorporated into a

3 programmable logic integrated circuit; and

4   including in the layout a watchdog timer circuit.

1   20. The method of claim 19 further comprising:

2   including signal lines in the layout of the embedded processor stripe to be coupled

3 to signal lines of a programmable logic portion of the programmable logic integrated circuit.

1   21. The method of claim 19 wherein the layout is designed to be positioned at

2 an edge of the programmable logic integrated circuit.

1   22. A circuit comprising:

2   a programmable logic integrated circuit comprising an embedded processor

3 portion and a programmable logic portion, wherein the embedded processor portion includes a

4 watchdog timer circuit; and

5   an external configuration source integrated circuit, coupled to the programmable

6 logic integrated circuit, storing configuration information for the programmable logic integrated

7 circuit, wherein when the watchdog timer circuit asserts a triggered signal output due to not

8 reloading the watchdog timer circuit within a timeout period, configuration data is loaded from

9 the external configuration source into the programmable logic integrated circuit.

1 23. The circuit of claim 22 wherein the external configuration source is a

2 nonvolatile memory.

1 24. The circuit of claim 22 wherein the watchdog timer circuit is reloaded by

2 periodically loading a reload register of the watchdog timer with one or more magic values.

1 25. The circuit of claim 22 wherein a configuration of the programmable logic

2 portion of the programmable logic integrated circuit is held using volatile memory cells.

1 26. The circuit of claim 25 wherein the volatile memory cells are SRAM cells.

1 27. The circuit of claim 22 wherein configuration data from the external

2 configuration source is used to configure the embedded processor portion and programmable

3 logic portion of the programmable logic integrated circuit.

1 28. The circuit of claim 22 wherein the configuration is transferred serially

2 from the external configuration source to the programmable logic integrated circuit.

1 29. The circuit of claim 22 wherein the watchdog timer circuit is not reloaded

2 due to a software failure occurring within the embedded processor portion of the programmable

3 logic integrated circuit.

1 30. The circuit of claim 22 wherein the watchdog circuit is not reloaded due to

2 a power supply problem.

1 31. A programmable logic integrated circuit comprising:

2 a programmable logic portion of the integrated circuit comprising a plurality of

3 logic array blocks, configurable to perform user logic, wherein the logic array blocks are

4 arranged in rows and columns; and

5 an embedded processor portion of the integrated circuit, coupled to the

6 programmable logic portion, comprising a watchdog timer circuit which is triggered if a count

7   register of the watchdog timer circuit is permitted to count to a final value before the count

8   register is reloaded.

1   32.   The programmable logic integrated circuit of claim 31 wherein triggering

2   of the watchdog timer circuit is avoided when the watchdog timer circuit is periodically

3   reloaded, before a timeout period, by writing a magic value to a reload register.

1   33.   The programmable logic integrated circuit of claim 32 wherein the timeout

2   period is a time it takes for the watchdog timer circuit to count from an initial value to the final

3   value.

1   34.   The programmable logic integrated circuit of claim 31 wherein the

2   plurality of logic array blocks are configured by programming SRAM memory cells.

1   35.   The programmable logic integrated circuit of claim 31 wherein the

2   plurality of logic array blocks are configured by programming volatile memory cells.

1   36.   The programmable logic integrated circuit of claim 31 wherein the

2   watchdog timer circuit comprises a reload register and a control register.

1   37.   The programmable logic integrated circuit of claim 31 wherein each logic

2   array block comprises a look-up table circuit.

1   38.   The programmable logic integrated circuit of claim 31 wherein after the

2   watchdog timer circuit is triggered, a reset circuit of the programmable logic integrated circuit

3   effects loading of configuration data from an external source to reconfigure the programmable

4   logic and embedded processor position of integrated circuit.

1   39.   The programmable logic integrated circuit of claim 31 wherein the

2   embedded processor portion further comprises a central processing unit and an embedded

3   processor memory block, coupled together using a first bus.

1   40.   The programmable logic integrated circuit of claim 39 wherein the

2   watchdog timer circuit is also coupled to the first bus.

26

1   41.   The programmable logic integrated circuit of claim 39 wherein the

2 embedded processor further comprises a second bus, through which the memory block is coupled

3 to the programmable logic portion of the integrated circuit.

1   42.   The programmable logic integrated circuit of claim 39 wherein the

2 external source is a Flash memory, EPROM memory, nonvolatile memory, or serial memory.

1   43.   The programmable logic integrated circuit of claim 38 wherein the

2 configuration data is transferred to the programmable logic integrated circuit by using a serial

3 stream of bits.

1   44.   A method of operating a programmable logic integrated circuit

2 comprising:

3   clocking a watchdog timer circuit to advance a count register of the watchdog

4 timer circuit;

5   loading a first magic value into a reload register of the watchdog timer circuit,

6 which resets the count register to an initial value;

7   after loading the first magic value, loading a second magic value into the reload

8 register, which causes the count register to reset the initial value; and

9   after loading the first magic value into the reload register, loading a value other

10 than the second magic value into the reload register, which causes the watchdog timer circuit to

11 generate a triggered signal.

1   45.   The method of claim 44 further comprising:

2   receiving the triggered signal in a reset logic block of the integrated circuit, which

3 causes a reloading of configuration data from an external source into the integrated circuit.

1   46.   The method of claim 45 wherein the configuration data is used to

2 configure an embedded processor portion and a programmable logic portion of the integrated

3 circuit.

1   47.   The method of claim 45 wherein the watchdog timer circuit is located in

2   an embedded processor portion and the reset logic block is located in a programmable logic

3   portion of the integrated circuit.

1   48.   The method of claim 44 further comprising:

2   allowing the count register of the watchdog timer to advance to a final value

3   before the first or second magic values are loaded, which causes the watchdog timer circuit to

4   generate the triggered signal.

1   49.   The method of claim 44 wherein the initial value is 0.

1   50.   The method of claim 44 wherein the initial value is a value other than 0.

1   51.   The method of claim 44 wherein the first magic value is different from the

2   second magic value.

1   52.   The method of claim 48 wherein the final value is user-selectable.

1   53.   The method of claim 48 wherein the final value is the maximum count

2   permitted by the count register.

1   54.   The method of claim 44 wherein in a debug mode, the count register does

2   not advance.